AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A semiconductor device, comprising:

a first carrier substrate;

a first semiconductor chip mounted face down on the first carrier substrate;

a second semiconductor chip mounted face down on a reverse face of the first carrier substrate;

a second carrier substrate;

a third semiconductor chip mounted on the second carrier substrate; and

protruding electrodes connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first semiconductor chip such that a gap is created between the second carrier substrate and the first semiconductor chip;

wherein the third semiconductor chip comprises a structure in which a plurality of chips are stacked.

2. (Cancelled)

3. (Original) The semiconductor device according to Claim 1, further comprising a sealant for sealing the third semiconductor chip.

4. (Original) The semiconductor device according to Claim 3,

wherein the sealant further comprises a molded resin.

5. (Original) The semiconductor device according to Claim 4,

wherein a position of a sidewall of the sealant coincides with a sidewall of the second carrier substrate.

6-7. (Cancelled)

8. (Original) The semiconductor device according to Claim 1,

wherein the first carrier substrate on which the first semiconductor chip and the second semiconductor chip are mounted further comprises a flip-chip-mounted ball grid array, and

wherein the second carrier substrate on which the third semiconductor chip is mounted further comprises at least one of a mold-sealed ball grid array and a chip size package.

9. (Cancelled)

10. (Original) The semiconductor device according to Claim 1,

wherein the third semiconductor chip comprises a structure in which a plurality of chips is arranged in parallel on the second carrier substrate.

11. (Currently Amended) An electronic device, comprising:

a first carrier substrate;

a first semiconductor chip mounted face down on at least one face of the first carrier substrate;

a second carrier substrate;

a second semiconductor chip mounted on the second carrier substrate;

a third semiconductor chip mounted on a reverse face of the second carrier substrate; and

protruding electrodes bonding the second carrier substrate to the first carrier substrate;

wherein a gap is created between a bottom surface of the second carrier substrate opposite the third semiconductor chip and a top surface of the first semiconductor chip such that the second carrier substrate is spaced apart from the first semiconductor chip;

wherein the third semiconductor chip comprises a structure in which a plurality of chips are stacked.

12. (Currently Amended) A semiconductor device, comprising:

a carrier substrate;

a first semiconductor chip mounted face down on the carrier substrate;

a second semiconductor chip mounted face down on a reverse face of the carrier substrate;

a third semiconductor chip on which re-arrangement wiring line layers are formed on surfaces where electrode pads are formed; and

protruding electrodes connecting the third semiconductor chip to the carrier substrate so that the third semiconductor chip is held above and spaced apart from the first semiconductor chip such that a gap is created between the third semiconductor chip and the first semiconductor chip.

13. (Currently Amended) An electronic device, comprising:

a first carrier substrate;

a first electronic part mounted on the first carrier substrate;

a second electronic part mounted on a reverse face of the first carrier substrate;

a second carrier substrate;

a third electronic part mounted on the second carrier substrate;

protruding electrodes connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above and spaced apart from the first electronic part such that a gap is created between the second carrier substrate and the first electronic part; and

a sealant for sealing the third electronic part;

wherein the third semiconductor chip comprises a structure in which a plurality of chips are stacked.

14-17. (Cancelled)